

AMENDMENTS TO THE CLAIMS

1. (currently amended) A mixer circuit comprising:

a first mixer stage comprising a first transmission gate and a second transmission gate, wherein the first transmission gate includes complementary transistors and is coupled with a first mixed signal terminal and first and second local oscillator (LO) signal terminals, and the second transmission gate includes complementary transistors and is coupled with a second mixed signal terminal and the first and second LO signal terminals;

a second mixer stage comprising a third transmission gate and a fourth transmission gate, wherein the third transmission gate includes complementary transistors and is coupled ~~with,~~ with the first transmission gate, the first mixed signal terminal and the first and second LO signal terminals so as to operate out of phase with the first transmission gate, and the fourth transmission gate includes complementary transistors and is coupled with the third transmission gate, the second mixed signal terminal and the first and second LO signal terminals so as to operate out of phase with the second transmission gate;

a first base band signal terminal coupled with the first and second transmission gates; and

a second base band signal terminal coupled with the third and fourth transmission gates;

wherein the mixer circuit processes signals so as to provide for at least one of:

mixing a first base band signal communicated to the first and second base band signal terminals with a differential LO signal communicated to the first and second LO signal terminals to create a first mixed signal; and

extracting a second base band signal from a second mixed signal communicated to the first and second mixed signal terminals ~~signal~~ using the LO signal communicated to the first and second LO signal terminals.

2. (original) The mixer circuit of claim 1, wherein the first, second, third and fourth transmission gates comprise CMOS transmission gates each having an n-type field-effect transistor (FET) having a source terminal and a drain terminal coupled, respectively, with a source terminal and a drain terminal of a p-type FET.

3. (original) The mixer circuit of claim 2, wherein source terminals of the n-type and p-type transistors of the first and third transmission gates are coupled with the first mixed signal terminal and source terminals of the n-type and p-type transistors of the second and fourth transmission gates are coupled with the second mixed signal terminal.

4. (original) The mixer circuit of claim 3, wherein gate terminals of the n-type FETs of the first and fourth transmission gates and gate terminals of the p-type FETs of the second and third transmission gates are coupled with the first LO signal terminal; and

gate terminals of the n-type FETs of the second and third transmission gates and gate terminals of the p-type FETs of the first and fourth transmission gates are coupled with the second LO signal terminal.

5. (original) The mixer circuit of claim 2, wherein drain terminals of the n-type and p-type transistors of the first and second transmission gates are coupled with the first base band signal terminal and drain terminals of the n-type and p-type transistors of the third and fourth transmission gates are coupled with the second base band signal terminal.

6. (original) The mixer circuit of claim 1, wherein the circuit is embodied on an integrated circuit such that the first, second, third and fourth transmission gates are substantially physically symmetric with the first and second transmission gates having the same orientation with respect to each other and the third and fourth transmission gates having the same orientation with respect to each other.

7. (original) The mixer circuit of claim 6, wherein the integrated circuit comprises a complementary metal-oxide semiconductor integrated circuit.

8. (original) The mixer circuit of claim 1, further comprising a balanced-unbalanced device coupled with a LO circuit and the first and second LO signal terminals.

9. (original) The mixer circuit of claim 1, further comprising a balanced-unbalanced device coupled with a single-ended mixed signal terminal and the first and second mixed signal terminals.

10. (original) The mixer of claim 9, wherein the single-ended mixed signal terminal receives the second mixed signal from an external mixed signal source.

11. (original) The mixer of claim 9, wherein the first mixed signal is communicated to a remote receiver via the single-ended mixed signal terminal.

12. (currently amended) A mixer circuit comprising:
a first balanced-unbalanced device coupled with an oscillator circuit, the first balanced-unbalanced device being further coupled with a reference voltage signal and first and second local oscillator (LO) signal terminals;

a second balanced-unbalanced device coupled with a single-ended mixed signal terminal and further coupled with first and second differential mixed signal terminals, the second balanced-unbalanced device being still further coupled with a ground voltage reference;

a first mixer stage comprising a first transmission gate and a second transmission gate, wherein the first transmission gate is coupled with the first differential mixed signal terminal and the first and second local oscillator (LO) signal terminals, and the second transmission gate is coupled with the second differential mixed signal terminal and the first and second LO signal terminals;

a second mixer stage comprising a third transmission gate and a fourth transmission gate, wherein the third transmission gate is coupled with the first differential mixed signal terminal and the first and second LO signal terminals so as to operate out of phase with the first transmission gate, and the fourth transmission gate is coupled with the second differential mixed

signal terminal and the first and second LO signal terminals so as to operate out of phase with the second transmission gate; and

a first base band signal terminal coupled with the first and second transmission gates; and

a second base band signal terminal coupled with the third and fourth transmission gates.

13. (original) The mixer circuit of claim 12, wherein the first and second base band signal terminals comprise first and second base band input signal terminals, such that a base band signal communicated to the first and second base band input signal terminals is mixed with a differential LO signal communicated from the oscillator circuit to the first and second LO signal terminals via the first balanced-unbalanced device to generate a differential mixed signal, which is communicated to the second balanced-unbalanced device to generate a single-ended mixed signal.

14. (original) The mixer circuit of claim 12, wherein the single-ended mixed signal terminal comprises a single-ended mixed input signal terminal, such that a differential mixed signal is generated as a result of a single-ended mixed signal being communicated to the second balanced-unbalanced device via the single-ended mixed input signal terminal, wherein the differential mixed signal is communicated to the first and second mixed signal terminals from the second balanced and unbalanced device, and

wherein the differential mixed signal is processed by the first and second mixer stages to extract a differential base band signal from the differential mixed signal using a differential LO

signal communicated from the oscillator circuit to the first and second LO signal terminals via the first balanced-unbalanced device.

15. (original) The mixer circuit of claim 12, wherein the first, second, third and fourth transmission gates comprise CMOS transmission gates each having an n-type field-effect transistor (FET) having a source terminal and a drain terminal coupled, respectively, with a source terminal and a drain terminal of a p-type FET.

16. (original) The mixer circuit of claim 15, wherein source terminals of the n-type and p-type transistors of the first and third transmission gates are coupled with the first mixed signal terminal and source terminals of the n-type and p-type transistors of the second and fourth transmission gates are coupled with the second mixed signal terminal.

17. (original) The mixer circuit of claim 15, wherein gate terminals of the n-type FETs of the first and fourth transmission gates and gate terminals of the p-type FETs of the second and third transmission gates are coupled with the first LO signal terminal; and

gate terminals of the n-type FETs of the second and third transmission gates and gate terminals of the p-type FETs of the first and fourth transmission gates are coupled with the second LO signal terminal.

18. (original) The mixer circuit of claim 15, wherein drain terminals of the n-type and p-type transistors of the first and second transmission gates are coupled with the first base band

signal terminal and drain terminals of the n-type and p-type transistors of the third and fourth transmission gates are coupled with the second base band signal terminal.

19. (original) The mixer circuit of claim 12, wherein the circuit is embodied on an integrated circuit such that the first, second, third and fourth transmission gates are substantially physically symmetric with the first and second transmission gates having the same orientation with respect to each other and the third and fourth transmission gates having the same orientation with respect to each other.

20. (original) The mixer circuit of claim 19, wherein the integrated circuit comprises a complementary metal-oxide semiconductor integrated circuit.

21. (original) The mixer circuit of claim 20, wherein the first and second balanced-unbalanced devices each comprise a transformer wherein at least one coil of each transformer comprises a center tap for applying a voltage reference.

22. (currently amended) In a differential mixer circuit comprising a first mixer stage having first and second signal paths coupled with first and second mixed signal terminals and first and second local oscillator (LO) signal terminals; a second mixer stage having first and second signal paths coupled with the first and second mixed signal terminals and the first and second LO signal terminals so as to operate out of phase with the first mixer stage; a first base

band signal terminal coupled with the first mixer stage; and a second base band signal terminal coupled with the second mixer stage, an improvement comprising:

implementing the first and second mixer stages using a signal-path circuit, wherein the signal-path circuit implementing each signal path for each mixer stage comprises at least a first device and a second ~~device~~ ~~devices~~, device, the first device and the second device being complementary to each other,

wherein the first device, having a first set of resistance characteristics, is coupled with ~~a~~ the second device, having a second set of resistance characteristics, the first and second resistance characteristics being inversely related to one another, thereby increasing a linear operation range of the mixer circuit and raising a one decibel compression point of the mixer circuit.

23. (original) The mixer circuit of claim 22, wherein each signal-path circuit implementing the first and second signal paths of the first and second mixer stages comprises a transmission gate.

24. (original) The mixer circuit of claim 23, wherein each transmission gate comprises a CMOS transmission gate comprising an n-type field-effect transistor (FET) having a source terminal and a drain terminal coupled, respectively, with a source terminal and a drain terminal of a p-type FET.

25. (original) The mixer circuit of claim 24, wherein the source terminals of the n-type and p-type transistors of a first transmission gate of the first mixer stage and a first transmission gate of the second mixer stage are coupled with the first mixed signal terminal and source terminals of the n-type and p-type transistors of a second transmission gate of the first mixer stage and a second transmission gate of the second mixer stage are coupled with the second mixed signal terminal.

26. (original) The mixer circuit of claim 24, wherein gate terminals of the n-type FETs of the first transmission gate of the first mixer stage and the second transmission gate of the second mixer stage and gate terminals of the p-type FETs of the second transmission gate of the first mixer stage and the first transmission gate of the second mixer stage are coupled with the first LO signal terminal; and

gate terminals of the n-type FETs of the second transmission gate of the first mixer stage and the first transmission gate of the second mixer stage and gate terminals of the p-type FETs of the first transmission gate of the first mixer stage and the second transmission gate of the second mixer stage are coupled with the second LO signal terminal.

27. (original) The mixer circuit of claim 24, wherein drain terminals of the n-type and p-type transistors of the first mixer stage are coupled with the first base band signal terminal and drain terminals of the n-type and p-type transistors of the second mixer stage are coupled with the second base band signal terminal.

28. (original) The mixer circuit of claim 22, wherein the circuit is embodied on an integrated circuit.